REMARKS

Claims 1-7 remain active in the application. Claims 1, 3 and 7 have been amended. Claims 8-20 were previously withdrawn from consideration.

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Applicants' Admitted Prior Art [AAPA] Figure 1 in combination with Chang et al. (U.S.P. 6,696,717) [Chang].

Applicants summarize the arguments presented in the previous Amendment filed on January 18, 2007.

Applicants contend that Chang's cell teaches having three conductive layers: a) a first conductive layer 116; b) a second conductive layer 124; and c) a third conductive layer 110. Applicants submit that the dual material gate layers 12 and 13 taught by the present invention (in Figure 2) find no equivalency in the combination of AAPA with Chang. In order to clearly pinpoint the differences between AAPA combined with Chang from the structure taught by the present application, Applicants had presented in the previous Amendment submitted by the Applicants on January 18, 2007, a drawing appended to this Amendment to clarify the differences. The enclosed drawing showed three figures:

a) the Admitted Prior Art Figure 1 [AAPA], referred to in the Office Action;
b) the combination of AAPA-Chang cited by the Office Action to reject claims 1-7 under 35 U.S.C. 103(a); and
c) the structure taught by Applicants in Figure 2 of the present application, which Applicants deem to be their invention.

The combination of AAPA and Chang listed above in item b) teaches gate 1 and gate 2 made of different materials. Gate 1 is shown to be beside the spacer. The gate controlling the channel is made of one material only.

In contradistinction to AAPA-Chang, the structure taught by Applicants (listed above under item c)) teaches the gate controlling the channel comprised of Gate 2 and Gate 3 being made of two materials. Applicants submit that one skilled in the art would have no way of determining where exactly the gate material layers are to be placed within the structure combining AAPA with Chang.

Chang in his Figure 4 shows each of a plurality of gates labeled 127 (each comprised of gate 126a, gate spacer 126c and cap layer 126b) being exposed, a necessary requirement since each of the gate structures serves as a word line (see col. 3, lines 59-65). Applicants wonder how a structure having exposed gates 127 is now to be combined with AAPA, wherein the region labeled Gate 1 is fully embedded in an N+ doped polysilicon region.

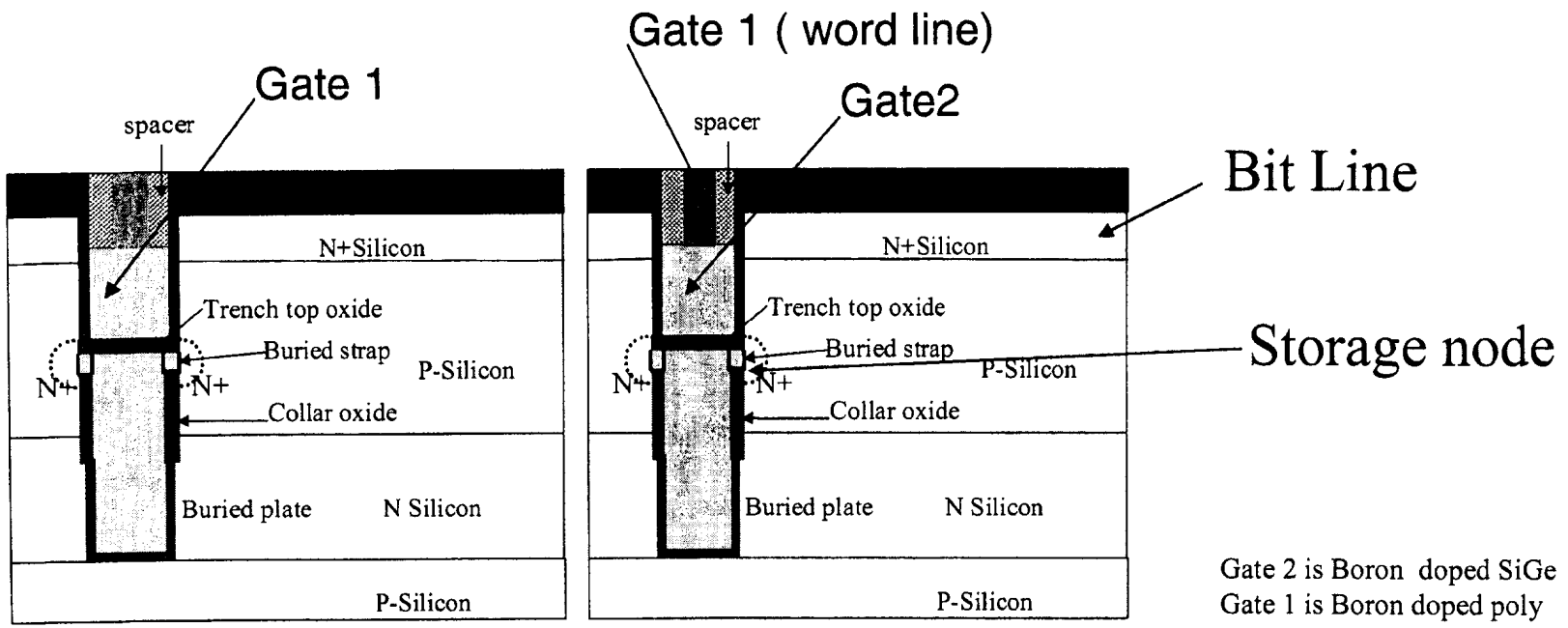
Applicants submit further that, when AAPA is combined with Chang, the resultant structure fails to achieve the objectives set by the Applicants and, consequently, would be inoperable since the dual material gate 1 and 2 taught by Chang are moot regarding where exactly to place the dual materials for the gate controlling the channel. The combination of AAPA-Chang arbitrarily positions a first material in Gate 1 beside the spacer and a second material anywhere within the region above the trench top oxide layer.

Applicants submit further that their invention is designed to provide a method for maintaining a low total leakage current while providing sufficient current drive for the vertical DRAM pass transistor (see Summary of the present invention). Chang, on the other hand, teaches how to prevent punch through, drain-induced barrier lowering (DIBL), and threshold voltage roll-over. Combining Chang with AAPA implies merging two incompatible structures which teaches away from the objectives set originally by Chang.

The present Office Action states that the feature upon which Applicants rely, namely "the gate controls a channel, the gate comprised of Gate 2 and Gate 3 being made of two materials" was not recited in the claims.

Applicants once again traverse the assertion made by the Office Action in its rejection of claims 1 to 7, and submit that the introduction of the limitation suggested by the Office Action is unnecessary and unwarranted.

Applicants are adding additional evidence in the form of arguments (that follow) and contend that Claims 1 through 7, as presented in the Amendment filed on January 18, 2007, sufficiently differ from the combination of AAPA and Chang.



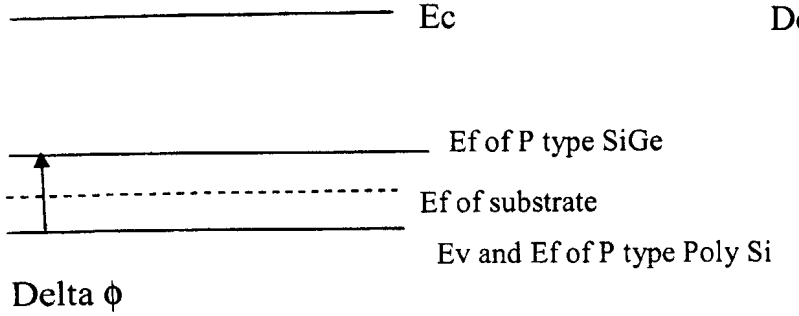
Gate 2 is Boron doped SiGe
Gate 1 is Boron doped poly

Prior art

Chang's

$$Vt = \phi m - \phi s - Qox/Cox + 2\psi B + (4\varepsilon siqNa\psi B)1/2/Cox$$

Threshold voltage difference between prior art and Chang's is Delta ϕ.



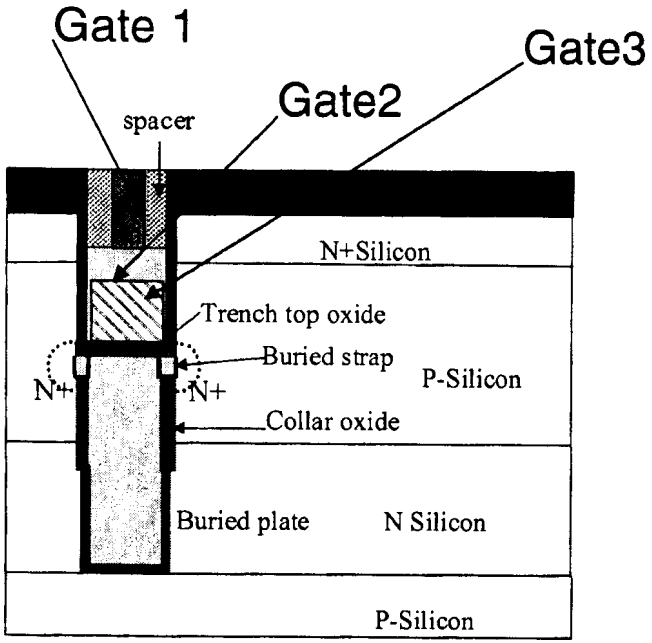
DRAM operation condition for Chang's invention

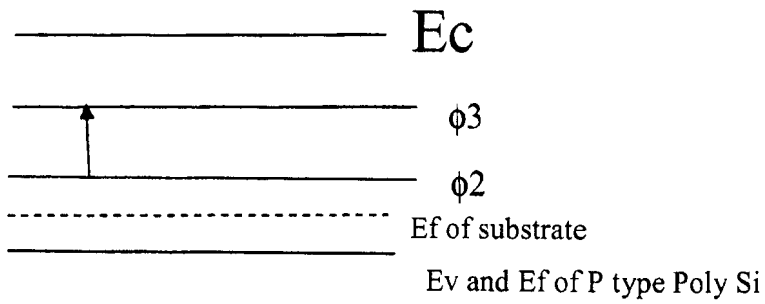
Case1: Bit Line =0, Word line =0 and storage node=1
Case 2: Bit Line =1, Word line =1 and storage node=low.

Case 1: Storage node is drain and Bit line is source.
Case 2: Bit line is drain and storage node is source.

The threshold voltage for the MOSFET is **same** for case 1 and case 2 because the gate material next to gate dielectric (114) is same material (116).

Band graph in our structure





The work function for gate material 2 is larger than material 3

DRAM operation condition for for our invention

Case1: Bit Line =0, Word line =0 and storage node=1
Case 2: Bit Line =1, Word line =1 and storage node=low.

Case 1: Storage node is drain and Bit line is source.
Case 2: Bit line is drain and storage node is source.

The threshold voltage in case 1 (Vt1) is larger than the threshold voltage in case 2(Vt2).
Vt1-Vt2= ϕ2- ϕ3.

The benefit to have asymmetric threshold voltage:
Low leakage at case 1 when the leakage is critical due to high Vt.
High write back current at case 2 due to low Vt at this case.

Advantage of the novel device structures

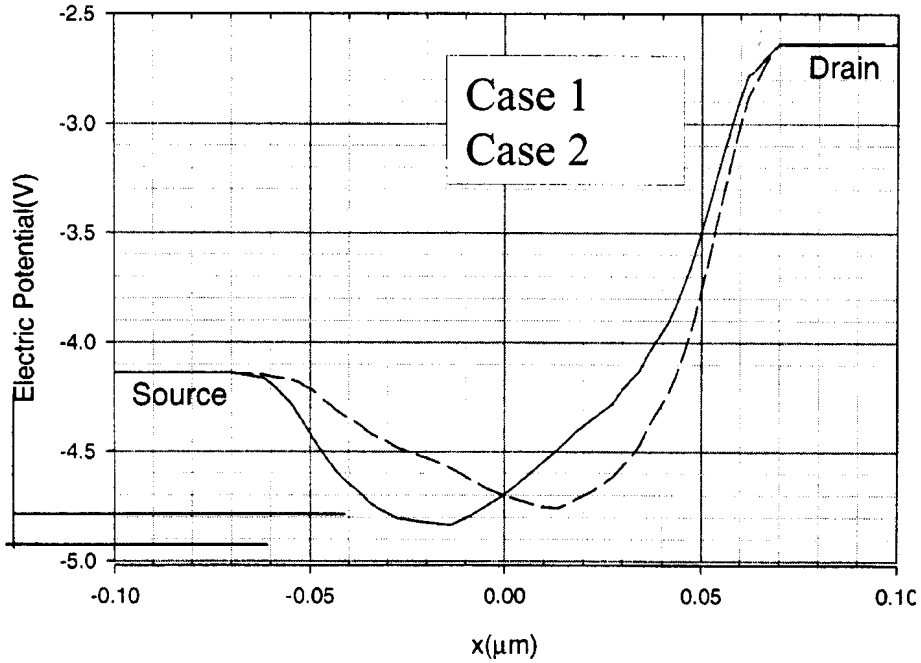
1)$\phi 1 > \phi 2$

In this case, V_t at the source side of the channel is larger than that of the drain side.

- Drain induced barrier lowering (DIBL) can be suppressed since the barrier height between the source and channel is increased with larger work function material at the source side.
- The electric field at the drain side is reduced when the device is at on-state, therefore, the hot carrier effect can be suppressed.
- The gate induced drain leakage current can suppressed due to smaller Vt at the drain side.

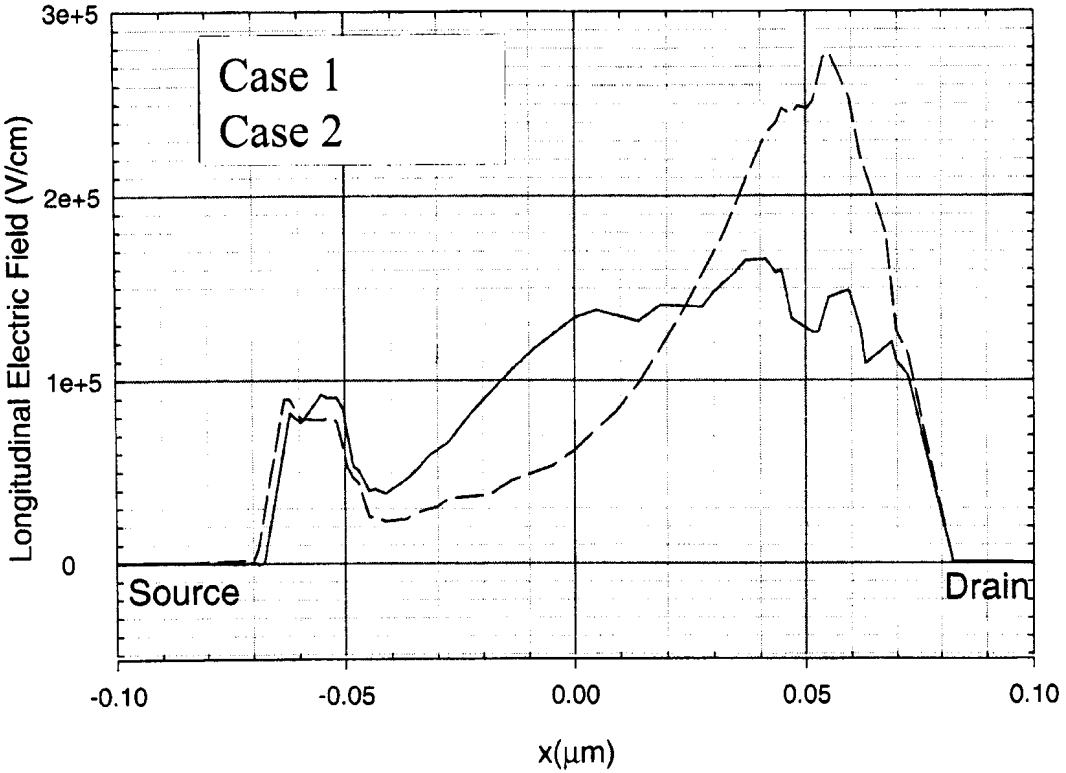
2) $\phi 1 > \phi 2$

In this case, the electric field at the drain side is increased when the device is at on-state, therefore, the hot carrier effect can be amplified. The device structure is useful in flash memory .



Simulated electric potential profiles along the channel for the dual gate work function device in the normal and reverse mode at V_{ds}=1.5V and V_{gs}=0V.

In Chang's invention, case 1 and 2 will be same.



Simulated longitudinal electric field along the channel for the dual work function gate NMOSFET in the normal and reverse state.

In Chang's case, case 1 and 2 will be same

In spite of the foregoing, and in order to advance the prosecution of the present application, Applicants have opted to include the aforementioned limitations in claims 1 and 7, as suggested by the Examiner and confirmed in a telephone conversation between the Examiner and Applicants' representative.

Thus, Applicants believe that they have overcome the rejection of claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' prior art Figure 1 [AAPA] in view of Chang, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing, it is respectfully requested that all the outstanding objections and rejections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,

XIANGDONG CHEN ET AL.

By: _____

H. Daniel Schnurmann, Agent
Registration No. 35,791
Tel. No. (845) 894 2481